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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/516,713	12/01/2004	Wolfgang Schnitt	DE02 0137 US	6751

65913 7590 03/19/2007  
NXP, B.V.  
NXP INTELLECTUAL PROPERTY DEPARTMENT  
M/S41-SJ  
1109 MCKAY DRIVE  
SAN JOSE, CA 95131

EXAMINER
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LIU, BENJAMIN T

ART UNIT	PAPER NUMBER
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2826

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/516,713	<b>Applicant(s)</b> SCHNITT ET AL.	
	<b>Examiner</b> Benjamin T. Liu	<b>Art Unit</b> 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 December 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

*Minhloan Tran*

**Minhloan Tran**  
**Primary Examiner**  
**Art Unit 2826**

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

### *Claim Rejections - 35 USC § 102(b)*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-10 are rejected under 35 U.S.C 102(b) as being anticipated by Zhang (5,886,364).

With regard to claim 1, figures 3A-3D of Zhang discloses a semiconductor-on-insulator (SOI) device, comprising: at least one isolating layer 31 made of a dielectric material (glass); at least one silicon substrate 34 arranged on the isolating layer 31; at least one component (40, 41, 42) integrated planarly in the silicon substrate 34, which component (40, 41, 42) has at least one slightly doped zone 41 laterally situated between a first highly doped zone 40 and a second highly doped zone 42; as well as at least a first planar metallization region (32, aluminum) arranged between the isolating layer 31 and the component (40, 41, 42), between the isolating layer 31 and the slightly doped zone 41 of the component (40, 41, 42), characterized in that at least a second planar, metallization region (38, aluminum) is arranged on the side of the silicon

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substrate 34 facing away from the isolating layer 31, in the area of the component (40, 41, 42) in the area of the slightly doped zone 41 of the component (40, 41, 42).

With regard to claim 2, figures 3A-3D of Zhang discloses the limitation, characterized in that a silicon substrate 34 comprising the component is fixed onto the isolating layer 31 with at least one fixing medium 33, with an adhesive layer 33.

With regard to claim 3, figures 3A-3D of Zhang discloses the limitation, characterized in that the first highly doped zone 40, the slightly doped zone 41 and the second highly doped zone 42 form at least one bipolar pnp transistor in the component (40, 41, 42); and the slightly doped zone 41 of the component (40, 41, 42) forms the n-doped region 41 of the pnp transistor (40, 41, 42).

With regard to claim 4, figures 3A-3D of Zhang discloses the limitation, characterized in that the first metallization region 32 is embedded in at least a first oxide-based passivation layer 33.

With regard to claim 5, figures 3A-3D of Zhang discloses the limitation, characterized in that on the side of the component (40, 41, 42) facing the isolating layer 31, at least one oxide layer (37, silicon oxide) borders on at least the component (40, 41, 42) or on the first passivation layer 33.

With regard to claim 6, figures 3A-3D of Zhang discloses the limitation, characterized in that between the component (40, 41, 42) and the second metallization region 38 at least a second buried oxide-based passivation layer 46 is arranged.

With regard to claim 7, figures 3A-3D of Zhang discloses the limitation, at least one isolating layer 31 made of a dielectric material (glass) is provided with at least one

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silicon substrate 34 using adhesive means; at least one component (40, 41, 42), having at least one slightly doped zone 41 laterally situated between a first highly doped zone 40 and a second highly doped zone 42, is planarly integrated in the silicon substrate 34; and at least a first planar metallization region 32 is arranged between the isolating layer 31 and the slightly doped zone 41 of the component (40, 41, 42), characterized in that at least a second planar metallization region 38 is provided on the side of the silicon substrate 34 facing away from the isolating layer 31, in the area of the slightly doped zone 41 of the component (40, 41, 42).

With regard to claim 8, figures 3A-3D of Zhang discloses the limitation, characterized in that the first metallization region 32 is embedded in at least a first oxide-based passivation layer 33.

With regard to claim 9, figures 3A-3D of Zhang discloses the limitation, characterized in that at least a second buried oxide-based passivation layer 46 is arranged between the component (40, 41, 42) and the second metallization region 38.

With regard to claim 10, figures 3A-3D of Zhang discloses the application of at least a first planar metallization region 32 as well as at least a second planar metallization region 38 to electrically shield, on both sides, the at least one component (40, 41, 42) incorporated in the silicon substrate 34 of a SOI device, to electrically shield, on both sides, the at least one slightly doped zone 41 of the component (40, 41, 42). (Note abstract of Zhang)

### ***Conclusion***

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3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin T. Liu whose telephone number is (571) 272-6009. The examiner can normally be reached on Mon-Fri 9:30 AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue A. Purvis can be reached on 571 272 1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BTL

3/8/2007